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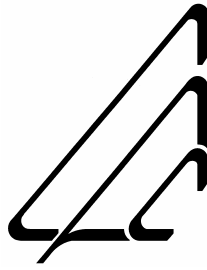
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ETC12™

Audio Interface for the ETPhone™ System

**Mezzanine Board
Technical Reference
Version 1.0**

email: support@cacdsp.com



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West Chester, PA (USA)

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1. ETC12 AUDIO INTERFACE FOR THE ETPHONE SYSTEM

1.1 ETPhone ETC12 Overview

1.1.1 ETC12 Introduction

This document specifies the characteristics of the ETC12, an ETPhone mezzanine board, with six Texas Instruments TLV320AIC23B CODECs with a total of 12 stereo audio channels, its memory, and the software libraries and drivers to support this board.



Figure 1-1: Front Panel ETP112

The front panel provides access to the following:

MMC Card	Additional Mountable File System
Head Phone	Channel 0 (LEFT) and Channel 1 (RIGHT) Output
Line In	Channel 0 (LEFT) and Channel 1 (RIGHT) Input
Microphone In	Mono Input
ETC12 Audio	12 Addition Audio Channels (See Pinout Below)
Control/Volume	Not Yet Supported



Figure 1-2: Back Panel ETP112

The back panel provides access to the following:

12 Volt Power Input	Power Supply Input
RS232	Serial Interface to/from ETPhone Foundation Board
E1/T1	Telecom Interface
USB	Supported in Future Releases as alternative interface
100BT	2-port Ethernet Switch

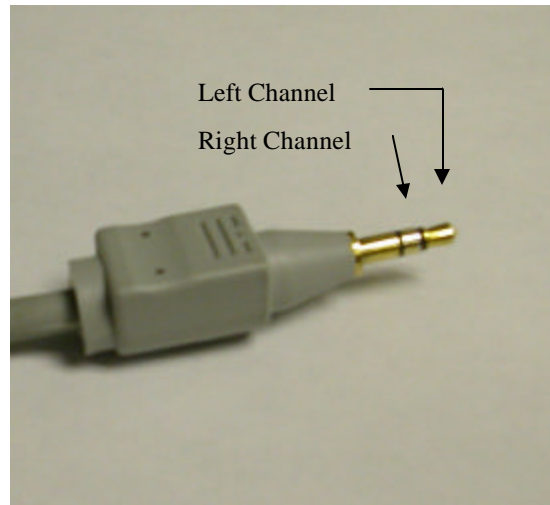


Figure 1-3: Audio Connector

1.1.2 ETC12 Top Level Description

The ETC12 is a mezzanine board for the ETPhone system. It contains the following major functional blocks:

- An ETPhone mezzanine bus interface
 - Six TLV320AIC23B CODECs with a total of 12 stereo audio channels
 - A RISC Bus connecting serial ports of the Xilinx® Spartan-III FPGA and other resources in the ETPhone system
 - A McBSP Interface connecting ETPhone's DSP to the FPGA and the CODECs.
 - 2 LEDs under FPGA program control
 - A global programmable frequency generator
 - A 64K x 8 EEPROM (for debug only)
 - A temperature sensor
- Software for Solaris, Windows 2000 and XP are provided, together with a software interface library to allow access to and control of the ETC12 from user-developed programs.
- Diagnostics are provided which are sufficient to verify correct operation of all functional blocks on the ETC12.

Figure 1-4 below shows the block diagram of the top level description.

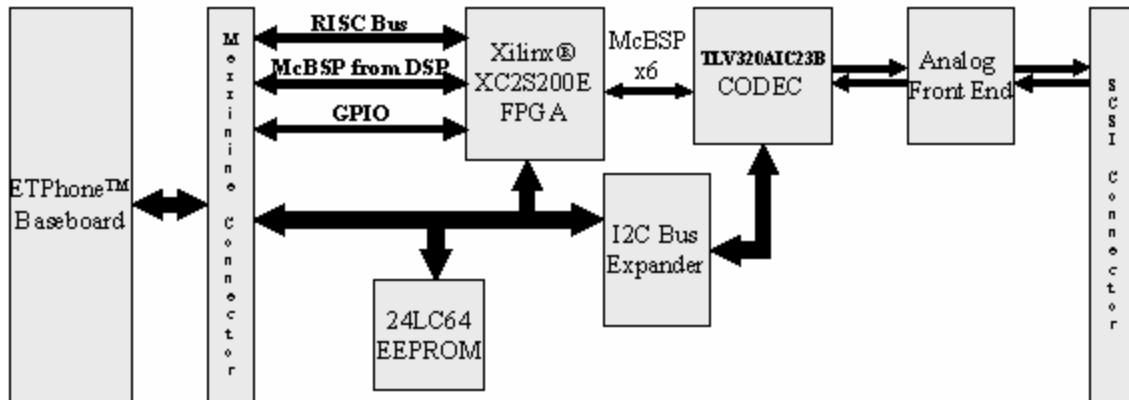


Figure 1-4: ETC12 Block Diagram

1.2 ETC12 Hardware Specification

The electrical hardware portions of the characteristics in Section 3 are elaborated in the following subsections.

1.2.1 ETPhone Mezzanine Interface

The ETPhone mezzanine connector provides the basic communication path between the baseboard and mezzanine board(s). Signals used by the ETC12 are grouped by function and discussed in subsequent sections.

Table 1-1: ETPhone Mezzanine Connector Pinout

Pin Number	Pin Name	I/O	Pin Number	Pin Name	I/O
1	+12V		2	+12V	
3	N/C		4	N/C	
5	RISC_TDMIN	I/O	6	GND	
7	RISC_TDMFRAME	I/O	8	TDM_MEZZ_CLK	O
9	GND		10	RISC_TDMOUT	I/O
11	RISC_TDMTEN	I/O	12	FPGA_BUSY/ MEZZ_CLK2	I/O
13	FPGA_DONE	I/O	14	GND	
15	FPGA_INIT_N/ MEZZ_CLK1	I/O	16	FPGA_PROGRAM_N	I/O
17	+3.3V		18	ATM_OUTP8	O
19	ATM_OUTP9	O	20	ATM_OUTP6	O

21	ATM_OUTP7	O	22	GND	
23	ATM_OUTP5	O	24	ATM_OUTP4	O
25	GND		26	ATM_OUTP2	O
27	ATM_OUTP3	O	28	ATM_OUTP0	O
29	ATM_OUTP1	O	30	GND	
31	ATM_INP11	I	32	ATM_INP10	I
Pin Number	Pin Name	I/O	Pin Number	Pin Name	I/O
33	GND		34	ATM_INP8	I
35	ATM_INP9	I	36	ATM_INP6	I
37	ATM_INP7	I	38	+3.3V	
39	ATM_INP5	I	40	ATM_INP4	I
41	GND		42	ATM_INP2	I
43	ATM_INP3	I	44	ATM_INP0	I
45	ATM_INP1	I	46	GND	
47	ATM_IOP1	I/O	48	ATM_IOP0	I/O
49	+3.3V		50	BCLKX2	I/O
51	BFSX2	I/O	52	BFDR2	I/O
53	BDR2	I	54	GND	
55	MEZZ_INT	I	56	BDX2	O
57	GND		58	RISC_BUF_RWN	O
59	BCLKR2	I/O	60	FPGA_CSN_N	I/O
61	RISC_BUF_BWEN0	O	62	GND	
63	RISC_BUF_BWEN1	O	64	RISC_BUF_OEN	O
65	GND		66	RISC_BUF_A23	O
67	WARM_RESETN	O	68	RISC_BUF_A21	O
69	RISC_BUF_A22	O	70	+3.3V	
71	RISC_BUF_A20	O	72	RISC_BUF_A19	O
73	GND		74	RISC_BUF_A17	O
75	RISC_BUF_A18	O	76	RISC_BUF_A15	O
77	RISC_BUF_A16	O	78	GND	
79	RISC_BUF_A14	O	80	RISC_BUF_A13	O
81	GND		82	RISC_BUF_A11	O
83	RISC_BUF_A12	O	84	RISC_BUF_A9	O
85	RISC_BUF_A10	O	86	GND	
87	RISC_BUF_A8	IO	88	RISC_BUF_A7	O
89	GND		90	RISC_I2C_SDA	I/O
91	RISC_BUF_A6	O	92	RISC_BUF_A5	O
93	RISC_I2C_SCL	O	94	GND	
95	RISC_BUF_A4	O	96	RISC_BUF_A3	O
97	+3.3V		98	RISC_BUF_A1	O
99	RISC_BUF_A2	O	100	RISC_BUF_A0	O
101	RISC_BUF_D15	I/O	102	GND	
103	RISC_BUF_D13	I/O	104	RISC_BUF_D14	I/O
105	GND		106	RISC_BUF_D12	I/O
107	RISC_BUF_D11	I/O	108	RISC_BUF_D10	I/O
109	RISC_BUF_D9	I/O	110	RISC_BUF_D8	I/O
111	RISC_BUF_D7	I/O	112	+3.3V	
113	GND		114	RISC_BUF_D6	I/O
115	RISC_BUF_D5	I/O	116	RISC_BUF_D4	I/O

117	RISC_BUF_D3	I/O	118	RISC_BUF_D2	I/O
119	RISC_BUF_D1	I/O	120	RISC_BUF_D0	I/O

Table 1-1 - ETPhone Mezzanine Connector Pinout (continued)

1.3 ETC12 CODECS

This section describes the basic operation of the Texas Instruments TLV320AIC23B CODECs, as they are integrated on the ETC12 mezzanine. Additional details on the operation of the CODECs may be found in the data sheet for the TLV320AIC23B CODEC which is available on CAC's FTP site (<ftp://ftp.cacdsp.com/pub/datasheets/ti/tlv320aic23b.pdf>).

1.3.1 Analog I/O

Gain Stages and Analog Characteristics

The figure below shows a functional diagram of the input and output gain stages for each of the 12 analog channels (2 channels per CODEC).

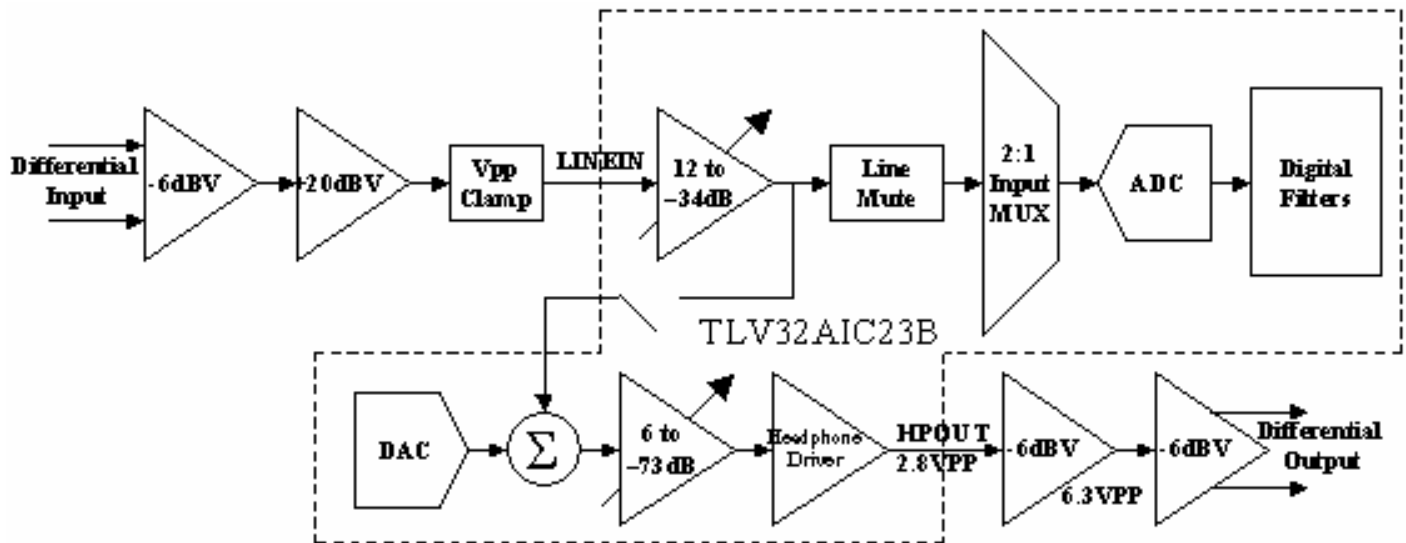


Figure 1-5: CODEC Channel Gain Stages

1.3.2 I/O Jumper Settings

For each of the 12 CODEC channels, there are two jumper blocks that configure the analog I/O circuitry. Figure 5 shows a diagram representing one section of the ETC12 PCB. This section is repeated 12 times in a 6 x 2 array on the board.

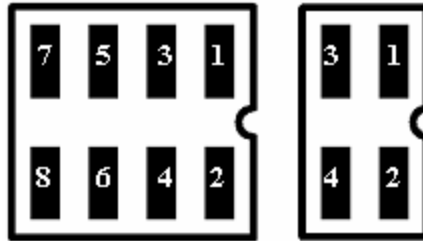


Figure 1-6: CODEC Channel Jumper PCB Section

One jumper block is 4x2 and is used as follows:

Table 1-2: 4x2 Jumper Block Settings

Jumper Pair	Function
1-2	Microphone Power
2-4	DC Coupled Input
5-6	DC Differential Input
3-5	AC Coupled Single-Ended Input
5-7	DC Coupled Single-Ended Input
6-8	Single-Ended Input

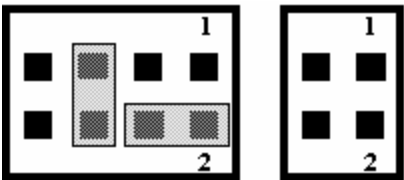
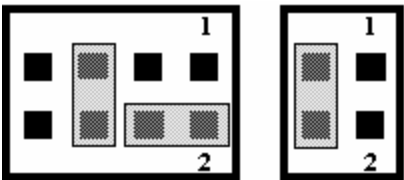
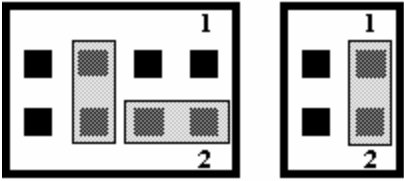
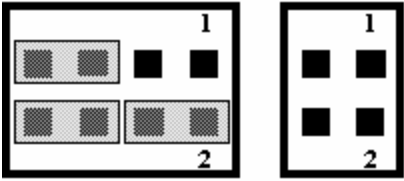
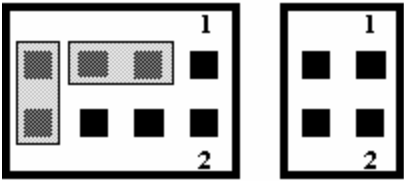
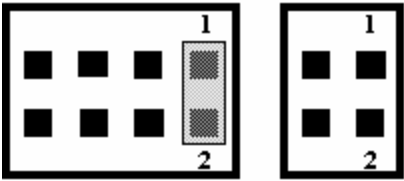
The second jumper block is 2x2 and is used as follows:

Table 1-3: 2x2 Jumper Block Settings

Jumper Pair	Function
1-2	Input Terminated with 604 Ohms Resistor
3-4	Single-Ended Output

Table 25 shows a variety of common jumper block configurations for reference.

Figure 1-7: CODEC Jumper Block Examples

DC Differential Input, Differential Output	DC Differential Input, Single-Ended Output
	
DC Differential Input, 600 Ohm Input	DC Single-Ended Input
	
AC Single-Ended Input	Microphone Power
	

1.3.3 ETPhone ETC12 System Audio Signals

The input and output audio channels as routed through the ETPhone system are differential, i.e. a pair of wires (+ and -) carry each signal. The numbering of the twelve channels start with 0 and ends with 11. Therefore, the input side of the first channel consists of the signals CIN00+ and CIN00-. Likewise, the outputs are labeled COUT00+ and COUT00-. In addition to the 48 signal wires, there are 19 pins that are either grounded or that have no-connections and a user-defined CLK signal, making a total of 68-pins. Standard 68-pin SCSI connectors, from AMP and standard 68-pin SCSI cables are used for interconnect of the audio components of the ETPhone system.

Figure 1-8 shows the AMP connector and to locate pin 1 for each type.

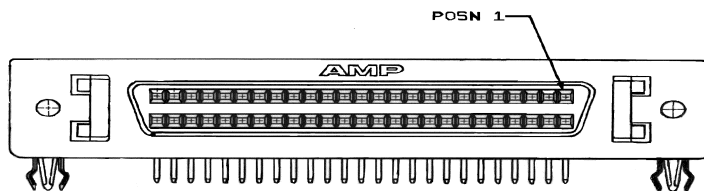


Figure 1-8: AMP SCSI connector

AMP connectors are used between the outside of the rear-panel and the audio patch panel. Standard external SCSI cables with thumbscrews or latches are used to make these connections.

Table 1-4: AMP SCSI Connector Pinout

Pin #	Signal Name	Pin #	Signal Name
1	COUT00-	35	OUT00+
2	CIN00+	36	CIN 00-
3	COUT01-	37	COUT01+
4	CIN 01+	38	CIN 01-
5	GND	39	GND
6	GND	40	GND
7	COUT02-	41	COUT02+
8	CIN 02+	42	CIN 02-
9	COUT03-	43	COUT03+
10	CIN 03+	44	CIN 03-
11	GND	45	GND
12	COUT04-	46	COUT04+
13	CIN 04+	47	CIN 04-
14	COUT05-	48	COUT05+
15	CIN 05+	49	CIN 05-
16	NC	50	NC
17	NC	51	NC
18	NC	52	NC
19	NC	53	External CLK
20	COUT06-	54	COUT06+
21	GND	55	GND
22	CIN 06+	56	CIN 06-
23	COUT07-	57	COUT07+
24	CIN 07+	58	CIN 07-
25	COUT08-	59	COUT08+
26	CIN 08+	60	CIN 08-
27	COUT09-	61	COUT09+
28	CIN 09+	62	CIN 09-
29	COUT10-	63	COUT10+
30	GND	64	GND
31	CIN 10+	65	CIN 10-
32	COUT11-	66	COUT11+
33	CIN 11+	67	CIN 11-
34	GND	68	GND

1.4 Display LEDs

The ETC12 has a bicolor status LED controlled by the Xilinx® FPGA. The ETC12 LED shows an green color once the FPGA is programmed.

1.5 Voltage and Temperature Sensor

The ETC12 has a NE1619 Voltage Monitor and temperature sensor. It monitors the +1.8V, +3.3AV, and +10AV supply voltages. The SMBus serial bi-directional data and the serial clock input, SDA and SCL pins are connected to the RISC I²C Bus Interface.

1.6 Mechanical Characteristics

The ETC12 is implemented as a mezzanine in the ETPhone system.

1.7 Power Consumption

The ETC12 requires +12V and + 3.3V. The power consumption requirement depends on the clock speed and the activity on the board. Power consumption has been empirically found to be as follows:

	Supply	Current	Power
ETPhone - ETC12	12V	0.7A	8.4W

1.8 Software

Software for Solaris, Windows XP and Window 2000 are provided, together with a host API to allow access to and control of the ETC12 from user-developed programs. Diagnostics are provided which are sufficient to verify correct operation of all functional blocks on the ETC12.

1.9 Reference Documents

1. Texas Instruments TLV320AIC23B Data Sheet.
2. Xilinx XC2S200E Series FPGA Data Sheet, September 1996.